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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,244	03/21/2001	David Glen Roe	70803	2001

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THE LAW OFFICE OF KIRK D. WILLIAMS
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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/814,244	ROE, DAVID GLEN	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5, 9, 12, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugawara (JP 10135786).

In reference to claim 1, Sugawara discloses in Figures 1 and 2 a circuit comprising: a first phase-locked loop (18): including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs (the output connected to block 14a), and a buffered reference clock output (the output of block 18g); and a second phase-locked loop circuit (20) including: an on-chip reference clock input and a second set of one or more phase-locked loop clock outputs (which are not specifically shown, but are considered to be an inherent part of any phase locked loop); wherein the buffered reference clock output of the first phase-locked loop circuit (18) is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit (20), see page 2 of the ABSTRACT lines 11-21. The same applies to claims 9, 18, and 20.

In reference to claim 3, Sugawara discloses in Figure 2 a buffer (18g) internal to the first phase locked loop (18), the buffer (18g) being electrically connected between

the off-chip reference clock input and the buffered reference output (see page 2 of the ABSTRACT lines 11-21).

In reference to claim 5, the circuit (10) of Sugawara is seen to be an application-specific integrated circuit (ASIC). The same applies to claims 12 and 19.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 8, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara (JP 10135786) in view of applicant's admitted prior art "Phase-Locked Loop," ASIC SA-27 Databook, Document No. SA 14-2214-02, IBM Corp., August 24, 1999, pp. 825-866.

In reference to claim 2, Sugawara discloses all of the limitations as mentioned above with reference to claims 1, 9, 18, and 20. However, Sugawara does not show that the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit includes at least two phase-locked loop clock outputs. The IBM reference discloses that the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit (PLL7SLIBE) includes at least two phase-locked loop clock outputs (PLLOUTA, PLLOUTB, PLLOUTC). Because it is well known to one skilled in the art that phase-locked loops can be designed to output multiple clock signals, it would have been obvious to one skilled in the art at the time of the invention

that the circuit of Sugawara could be modified simply by "tapping" the output or using multiple dividers as supported by the IBM reference. The same applies to claim 10.

In reference to claim 8, Sugawara discloses all of the limitations as mentioned above with reference to claims 1, 9, 18, and 20. However, Sugawara does not show that the off-chip reference clock input of the first phase-locked loop circuit is directly electrically coupled to a pad (I/O pads) of a chip. The IBM reference discloses on page 829 (in the Notes section) that the off-chip reference clock input of the first phase-locked loop circuit is directly electrically coupled to a pad (I/O pads) of a chip. The limitation is seen to be a design expedient dependent on the particular environment and the desired outcome. Therefore, it would have been obvious to one skilled in the art at the time of the invention that in the specified environment the off-chip reference clock input of the first phase-locked loop circuit (18) could have been directly electrically coupled to a pad (I/O pads) of a chip as evidenced by the IBM reference. The same applies to claim 14.

Claims 4, 6, 7, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara (JP 10135786) in view of Yabe et al. (U.S. Patent No. 5,698,876).

In reference to claim 4, Sugawara discloses all the limitations of the claim as mentioned above with reference to claims 1, 9, 18, and 20. However, Sugawara does not disclose that the first phase-locked loop circuit (18) and the second phase-locked loop circuit (20) are predefined library circuits. Yabe discloses in column 1, lines 37-40 that it is well known in the art that macro cells generally defined as library circuits are phase-locked loop circuits. Therefore, it would have been obvious to one skilled in the

art at the time of the invention that the phase-locked loop circuits of Sugawara could be defined as library circuits as supported by the Yabe reference. The same applies to claims 6, 7, 11, and 13.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara (JP 10135786) in view of Yabe et al. (U.S. Patent No. 5,698,876) and further in view of Anderson et al. (U.S. Patent No. 6,272,669).

In reference to claim 15, Sugawara in view of Yabe discloses all the limitations of the claim as mentioned above with reference to claims 1, 4, 6, 7, 9, 11, 13, 18, and 20. However, neither Sugawara nor Yabe discloses the method for designing a circuit for generating a first and a second clock reference signals called for in the claim. Anderson discloses in column 2, line 66 through column 3, line 4 a method for designing programmable semiconductor devices in a desired configuration. It would have been obvious to one skilled in the art at the time of the invention that the circuit of Sugawara could have been configured or "designed" using the method disclosed by Anderson for the advantage of being able to eliminate processes for deriving configuration data from high level design languages (see column 1, lines 30-34).

In reference to claim 16, the circuit (10) of Sugawara is seen to be an application-specific integrated circuit (ASIC).

In reference to claim 17, Sugawara discloses in Figure 2 that the first phase locked loop macro (18) includes a buffer (18g) connected between the off-chip reference clock input and the buffered reference clock output (see page 2 of the ABSTRACT lines 11-21).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC

CC

November 30, 2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800